

**Notice of References Cited**

Application/Control No.

10/813,433

Applicant(s)/Patent Under  
Reexamination  
KNOWLES, SIMON

Examiner

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Art Unit

2183

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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,798,239	09-2004	Douglass et al.	326/39
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Haynes et al., "Configurable Multiplier Blocks for use within an FPGA", IEEE Trans. Computers, Vol. 3, No.1, 1998, 6 pages
	V	Lodi et al., "A Flexible LUT-Based Carry Chain for FPGAs", 2003, pp.133-136
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.